Curriculum Vitæ

Maurizio Palesi

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Contacts

Name and title	Maurizio Palesi, PhD
Date of birth	June 10, 1974
City of birth	Catania, Italy
Status	Married with two kids
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Current and Past Positions

11/2016 - present	Associate Professor in Computer Engineering, Department of Electrical, Electronics and Computer Engineering, Università degli Studi di Catania, Catania, Italy
04/2014 - 10/2016	Associate Professor in Computer Engineering, Università degli Studi di Enna, KORE, Italy
11/2010 - 03/2014	Assistant Professor in Computer Engineering, Università degli Studi di Enna, KORE, Italy

Education

2003	PhD Degree in Computer Engineering, Università degli Studi di Catania, Italy
1999	Diploma di Laurea (five years degree) in Computer Engineering, (grade 110/110 e lode), Università degli Studi di Catania, Italy

Teaching

The teaching portfolio includes, computer architectures, embedded systems, fundamental of programming.

GIAN Global Initiative of Academic Networks

- **May 24 - 30, 2017**, Indian Institute of Technology Guwahati, Assam. Scalable On-chip Interconnects For Many-Core Systems (12 hours)

A.A. 2020/2021, Università degli Studi di Catania [21 CFU, 177 hours]

- Fundamentals of Programming (Electronics and Computer Engineering, 9 CFU, 79 hours)
- Computer Architectures (Computer Engineering, 3 CFU, 29 hours)
- Internet of Things based Smart Systems (Computer Engineering, 3 CFU, 29 hours)
- Internet of Thing and Big Data for Smart Spaces (Data Science for Management, 6 CFU, 40 hours)

A.A. 2019/2020, Università degli Studi di Catania [20 CFU, 164 hours]

- Fundamentals of Programming (Electronics and Computer Engineering, 9 CFU, 79 hours)
- Computer Architectures (Computer Engineering, 6 CFU, 50 hours)
- Internet of Things based Smart Systems (Computer Engineering, 5 CFU, 35 hours)

A.A. 2018/2019, Università degli Studi di Catania [21 CFU, 179 hours]

- Fundamentals of Programming (Electronics and Computer Engineering, 9 CFU, 79 hours)
- Computer Architectures (Computer Engineering, 6 CFU, 50 hours)
- Internet of Things based Smart Systems (Computer Engineering, 6 CFU, 50 hours)

A.A. 2017/2018, Università degli Studi di Catania [21 CFU, 179 hours]

- Fundamentals of Programming (Electronics and Computer Engineering, 9 CFU, 79 hours)
- Fixed and Mobile System Architectures Lab (Computer Engineering, 3 CFU, 25 hours)
- Internet of Things based Smart Systems (Computer Engineering, 6 CFU, 50 hours)

A.A. 2016/2017, Università degli Studi di Catania [18 CFU, 154 hours]

- Scalable On-chip Interconnects For Many-Core Systems May 24 - 30, 2017 @ Indian Institute of Technology Guwahati, Assam.
- Fundamentals of Programming (Electronics and Computer Engineering, 9 CFU, 79 hours)
- Fixed and Mobile System Architectures Lab (Computer Engineering, 3 CFU, 25 hours)
- Embedded Systems (Computer Engineering, 6 CFU, 50 hours)

A.A. 2015/2016, Università degli Studi di Enna, KORE [27 CFU, 180 hours]

- Introduction to Computer Science (Law, 2 CFU, 12 hours)
- Fundamentals of Programming (Computer and Telecommunication Engineering, 6 CFU, 54 hours)
- Computer Lab, (Psychological Science, 1 CFU, 6 hours)

- Computing Systems and Telecommunication (Defense Science, 6 CFU, 36 hours)
- Information Processing Systems (Business Economy, 6 CFU, 36 hours)
- Information Processing Systems (Economy and Business Management, 6 CFU, 36 hours)

A.A. 2014/2015, Università degli Studi di Enna, KORE [42 CFU, 270 hours]

- Introduction to computer science (Law, 2 CFU, 12 hours)
- Computer Science of Performance Evaluation of Sport Activity (Sciences of motor and sports activities, 6 CFU, 36 hours)
- Information Processing Systems (Social Service, 9 CFU, 54 hours)
- Fundamentals of Programming (Computer and Telecommunication Engineering, 6 CFU, 54 hours)
- Computer Lab, (Psychological Science, 1 CFU, 6 hours)
- Computing Systems and Telecommunication (Defense Science, 6 CFU, 36 hours)
- Information Processing Systems (Business Economy, 6 CFU, 36 hours)
- Information Processing Systems (Economy and Business Management, 6 CFU, 36 hours)

A.A. 2013/2014, Università degli Studi di Enna, KORE [27 CFU, 162 hours]

- Computer Science of Performance Evaluation of Sport Activity (Sciences of motor and sports activities, 6 CFU, 36 hours)
- Introduction to computer science (Law, 2 CFU, 12 hours)
- Computer Lab, (Psychological Science, 1 CFU, 6 hours)
- Computing Systems and Telecommunication (Defense Science, 6 CFU, 36 hours)
- Information Processing Systems (Business Wconomy, 6 CFU, 36 hours)
- Information Processing Systems (Economy and Business Management, 6 CFU, 36 hours)

A.A. 2012/2013, Università degli Studi di Enna, KORE [36 CFU, 216]

- Introduction to computer science (Law, 2 CFU, 12 hours)
- Computer Science of Performance Evaluation of Sport Activity (Sciences of motor and sports activities, 6 CFU, 36 hours)
- Information Processing Systems (Psychological science, 9 CFU, 54 hours)
- Computer Lab, (Psychological Science, 1 CFU, 6 hours)
- Computing Systems and Telecommunication (Defense Science, 6 CFU, 36 hours)
- Information Processing Systems (Business Economy, 6 CFU, 36 hours)
- Information Processing Systems (Economy and Business Management, 6 CFU, 36 hours)

A.A. 2011/2012, Università degli Studi di Enna, KORE [32 CFU, 192 hours]

- Introduction to computer science (Law, 2 CFU, 12 hours)
- Computer Science of Performance Evaluation of Sport Activity (Sciences of motor and sports activities, 6 CFU, 36 hours)

- Computer Science (Education Science, 6 CFU, 36 hours)
- Computing Systems and Telecommunication (Defense Science, 9 CFU, 54 hours)
- Information Processing Systems (Sociology and Social Policies, 2 CFU, 12 hours)
- Computer Lab, (Psychological Science, 1 CFU, 6 hours)
- Information Processing Systems (Economy and Business Management, 6 CFU, 36 hours)

A.A. 2010/2011, Università degli Studi di Enna, KORE [27 CFU, 162 hours]

- Methodologies for Internet based Storing Systems (Multimedia, 9 CFU, 54 hours)
- Computer Science (Psychological Science, 6 CFU, 36 hours)
- Information Processing Systems (Business Economy, 6 CFU, 36 hours)
- Information Processing Systems (Economy and Business Management, 6 CFU, 36 hours)

A.A. 2003/2004 a A.A. 2009/2010, Università degli Studi di Catania [6 CFU, 60 hours]

- Computer Architecture (Electronic Engineering, 6 CFU, 60 hours)

Master Student and PhD Student Supervision

- He has supervised more than 50 students for the Master Degree in Computer Engineering.
- He is *external co-supervisor* for Ph.D. in Electrical Engineering of students Mohd Shahrizal Bin Rusli and Munirah Binti Ab. Rahman, School of Graduate Studies, Universiti Teknologi Malaysia.
- He is in the *foreign evaluator panel* of the PhD program in Computer Engineering and Electrical Engineering at the Department of Electrical Engineering, COMSATS Institute of Information Technology (CIIT), Islamabad, Pakistan.
- He has been member of the commission for the international PhD exam of Francisco Triviño who defended a thesis entitled “Efficient, scalable, and cost-effective reconfiguration, virtualization, and fault tolerant support for on-chip networks” at Universidad de Castilla-La Mancha, Spain.
- He has been member of the commission for the international PhD exam of Francisco Gilabert Villamón who defended a thesis entitled “Design Space Exploration for Networks On-chip” at Universitat Politecnica de València, Spain.

Awards

- **2011 - Best Paper Award** Al-Dujaily, T. Mak, F. Xia, A. Yakovlev, M. Palesi. *Run-time Deadlock Detection in Networks-on-Chip using Coupled Transitive Closure Networks*. Design Automation and Test in Europe (DATE 2011). 14-18 March 2011, Grenoble, France.
- **2014 - HiPEAC Paper Award** M. Fattah, M. Palesi, P. Liljeberg, H. Tenhunen. *SHiFA: System-Level Hierarchy in Run-Time Fault-Aware Management of Many-Core Systems*. Design Automation Conference (DAC), 2014.

- **2014 - Outstanding Reviewer** To be within the top 10th percentile of reviewers for the Elsevier Computers & Electrical Engineering Journal, in terms of the number of manuscript reviews completed in the last two years.

Memberships

- **Dec. 2010 - present** Member of the European Network on High Performance and Embedded Architecture and Compilation (HiPEAC)
- **Dec. 2015 - present** IEEE Senior Membership is an honor bestowed only to those who have made significant contributions to the profession.

Seminars and Invited Speaker

Oct 31, 2021	International Conference on Circuits and Systems (IEEE ICCS 2021), Oct. 29-31, 2021, Chengdu, China
Feb. 15, 2017	On-Chip Approximate Communication for Energy Efficiency, *University of Southampton, UK.*
Dec. 14, 2009	Application Specific Routing Algorithms for Networks on Chip, *NEC Laboratories America, NJ, USA.*
Sep. 20, 2009 Oct. 2, 2009	Digital Signal Processing: Concepts and Theory, *Department of Electronics and Computer Engineering, School of Engineering, Jönköping University, Sweden.*
Jul 30, 2009	NoC Research Summary, *University of Nevada, USA.*
Sep. 25-26, 2008	Digital Signal Processing: Concepts and Theory, *Department of Electronics and Computer Engineering, School of Engineering, Jönköping University, Sweden.*
Sep. 28 Oct. 4, 2007	Introduction to DSP, *Department of Electronics and Computer Engineering, School of Engineering, Jönköping University, Sweden.*
Sep. 2006	Introduction to DSP, *Department of Electronics and Computer Engineering, School of Engineering, Jönköping University, Sweden.*
Jan 23, 2007	Routing Algorithms in Networks on Chip. *Universidad Politecnica de Valencia - DISCA, Escuela Técnica de Informática Aplicada.*
Oct. 2005	A Brief Introduction to Multiobjective Optimization Techniques. *School of Engineering, Jönköping University, Sweden.*
Oct. 2005	Some Key Issues in Embedded System Design. *Embedded Systems Laboratory, Department of Computer and Information Science, Linköping University, Linköping, Sweden.*

Services to the Research Community

Editor of Special Issues in International Journals

Co-Editor	Open Special Issue on Integrating Theory and Infrastructure into Online STEM Education	Computers & Education
Co-Editor	Special Issue on Integrating New Practices and Technology into STEM Education (Fangyang Shen, Irina Lyublinskaya, Yang (Cindy) Yi, Jun Zhang, Maurizio Palesi, Yi Han)	Integrating New Practices and Technology into STEM Education, Elsevier
Co-Editor	Special Issue on Communication-aware Designs and Methodologies for Reliable and Adaptable On-Chip AI SubSystems and Accelerators (Kun-Chih (Jimmy) Chen, Masoumeh (Azin) Ebrahimi, Maurizio Palesi, Tim Kogel)	IEEE Journal on Emerging and Selected Topics in Circuits and Systems
Co-Editor	Special Issue on Chip-scale Nanonetworks: Recent Trends, Emerging Technologies, Disruptive Applications (Sergi Abadal, Salvatore Monteleone, Kun-Chih Chen, Maurizio Palesi)	Nano Communication Networks, Elsevier
Co-Editor	Special Issue on Special Issue on Energy-Efficient Many-Core Embedded Systems and Architectures (Maurizio Palesi, Kun-Chih (Jimmy) Chen, Midia Reshadi)	Journal of Systems Architecture, Elsevier
Co-Editor	Special Issue on Intelligent Computing Systems and their Applications (Editors: Fangyang Shen, Mei Yang, Maurizio Palesi)	Computers and Electrical Engineering
Co-Editor	Special Issue on Towards Architectures & Applications of Mobile Wireless Sensor Networks (Editors: Yingtao Jiang, Ling Wang, Yuwang Yang, Maurizio Palesi, Terrence Mak)	International Journal of Distributed Sensor Networks
Co-Editor	Special Issue on Sustainable Processor Architectures and Applications (Editors: Fangyang Shen, Mei Yang, Maurizio Palesi)	Elsevier Microprocessors and Microsystems: Embedded Hardware Design
Co-Editor	Special Issue on Many-Core System-on-Chip: Architectures and Applications (Editors: Masoud Daneshtalab, Mohamed Bakhouya, Hassan Ghasemzadeh, Maurizio Palesi)	Elsevier Microprocessors and Microsystems: Embedded Hardware Design
Co-Editor	Special Issue on Fault-Tolerant and Reliable Interconnection Network for Parallel Computing	The Scientific World Journal, Hindawi

	Systems, (Editors: Masoumeh Ebrahimi, Maurizio Palesi, Zhiyi Yu, Diana Goehringer, Masoud Daneshtalab)	
Co-Editor	Special Issue on Energy Efficient Methods and Systems in the Emerging Cloud Era, (Editors: Pradip Bose, Mario Collotta, Masoud Daneshtalab, Maurizio Palesi)	Journal of Computer and System Sciences, Elsevier
Co-Editor	Special Issue on Network-on-Chip Architectures, (Editors: Masoud Daneshtalab, Terrence Mak, Maurizio Palesi)	Computers & Electrical Engineering Journal, Elsevier
Co-Editor	Special Issue on Emerging Research in Internet of Things (IoT) (Editors: Fangyang Shen, Lingjia Liu, Maurizio Palesi)	Elsevier Computers and Electrical Engineering
Co-Editor	Special Issue on Many-core Embedded Systems (Editors: Masoud Daneshtalab, Ahmed Hemani, Maurizio Palesi, Juha Plosila)	Elsevier Microprocessors and Microsystems: Embedded Hardware Design
Co-Editor	Special Issue on Emerging On-Chip Networks and Architectures (Editors: Maurizio Palesi, Masoud Daneshtalab, and Terrence Mak)	IET Computers & Digital Techniques
Co-Editor	Special Issue on Design Challenges for Many-core Processors (Editors: Masoud Daneshtalab, Maurizio Palesi, and Juha Plosila)	ACM Transactions on Embedded Computing Systems
Co-Editor	Special Section on Embedded Systems for Real-time Multimediain (Editors: Jian-Jia Chen and Maurizio Palesi)	ACM Transactions on Embedded Computing Systems
Co-Editor	Special Issue on Novel On-Chip Parallel Architectures and Software Support (Editors: Fangyang Shen, Mei Yang, Maurizio Palesi)	Elsevier, Journal of Parallel Computing
Co-Editor	Special Issue on On-Chip and Off-Chip Network Architectures (Editors: Maurizio Palesi and Josè Flich)	ACM Transactions on Embedded Computing Systems
Co-Editor	Special Issue on Emerging Computing Architectures and Systems in Elsevier (Editors: Fangyang Shen, Mei Yang, Maurizio Palesi)	Journal of Computers and Electrical Engineering
Co-Editor	Special Issue on Network-on-Chip Architectures and Design Methodologies (Editors: Maurizio Palesi, Shashi Kumar, Radu Marculescu)	Elsevier Microprocessors and Microsystems - Embedded Hardware Design
Co-Editor	Special Issue on Power-efficient, high performance General Purpose and Application Specific Computing Architectures (Editors: Mei Yang, Yingtao Jiang, Peng Liu, Maurizio Palesi)	International Journal of High Performance Systems Architecture

Co-Editor	Special Issue on Networks on Chip, VLSI Design Journal (Editors: Maurizio Palesi, Davide Bertozzi, Shashi Kumar)	Hindawi Publishing Corporation

Conference/Symposium/Workshop Organization

CF 2020	General Chair	ACM International Conference on Computing Frontiers 2020
NetACT 2019	General Chair	2nd International Conference on Networks & Advances in Computational Technologies
NoCArc 2016	General Co-Chair	9th International Workshop on Network on Chip Architectures. In conjunction with the 49th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO-49), October 15, 2016, Taipei, Taiwan.
MES 2016	General Co-Chair	4th ACM International Workshop on Manycore Embedded Systems. In conjunction with 43rd International Symposium on Computer Architecture (ISCA 2016). June 18-22, 2016 Seoul, Korea.
NoCArc 2015	General Co-Chair	8th International Workshop on Network on Chip Architectures. In conjunction with the 48th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO-48), December 6, 2015, Waikiki, Hawaii.
MES 2015	General Co-Chair	3rd ACM International Workshop on Manycore Embedded Systems. In conjunction with 42nd International Symposium on Computer Architecture (ISCA 2015). June 13-17, 2015 Portland, USA.
ESTIMedia 2014	General Chair	12th IEEE Symposium on Embedded Systems for Real-Time Multimedia. October 16-17, 2014, New Delhi, India.
NoCArc 2014	General Co-Chair	7th International Workshop on Network on Chip Architectures. In conjunction with the 47th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO-47), December 13, 2014, Cambridge, UK.
MES 2014	General Co-Chair	2nd ACM International Workshop on Manycore Embedded Systems. In conjunction with 41st International Symposium on Computer Architecture (ISCA 2014). June 14-18, 2014 Minneapolis, USA.

NoCArc 2013	General Co-Chair	6th International Workshop on Network on Chip Architectures. In conjunction with the 46th Annual IEEE/ACM Int. Symposium on Microarchitecture (MICRO-46), December 8, 2013, Davis, California, USA.
NoCArc 2012	General Co-Chair	5th International Workshop on Network on Chip Architectures. In conjunction with the 45th Annual IEEE/ACM Int. Symposium on Microarchitecture (MICRO-45), December 1-5, 2012, Vancouver, Canada.
MES 2013	General Co-Chair	1st ACM International Workshop on Manycore Embedded Systems. In conjunction with 40th International Symposium on Computer Architecture (ISCA 2013).
NoCArc 2011	General Co-Chair	4th International Workshop on Network on Chip Architectures. In conjunction with the 44th Annual IEEE/ACM Int. Symposium on Microarchitecture (MICRO-44), December 3-7, 2011, Porto Alegre, Brazil.
NoCArc 2010	General Co-Chair	3rd International Workshop on Network on Chip Architectures. In conjunction with the 43rd Annual IEEE/ACM International Symposium on Microarchitecture (MICRO-43), December 4, 2010, Atlanta, Georgia, USA.
NoCArc 2009	General Co-Chair	2nd International Workshop on Network on Chip Architectures. In conjunction with the 42nd Annual IEEE/ACM International Symposium on Microarchitecture (MICRO-42), December 12, 2009, New York City, USA.
NoCArc 2008	General Co-Chair	1st International Workshop on Network on Chip Architectures. In conjunction with the 41st Annual IEEE/ACM International Symposium on Microarchitecture (MICRO-41), November 8, 2008, Lake Como, Italy.

Positions as Chair

NOCS 2018 NOCS 2019	Special Sessions/Demos Chair	12th IEEE/ACM International Symposium on Networks-on-Chip (NOCS 2018) October 4-5, 2018, Torino, Italy
NOCS 2017	Publication Chair	11th International Symposium on Networks-on-Chip,

		Seoul, South Korea, October 19-20, 2017
CPS Week 2017	Publicity Chair	Cyber Physical Systems Week Conference, April 18-21, Pittsburgh, PA
Computing Frontiers 2017	Publicity Chair	Computing Frontiers, Siena, Italy, May 15-17, 2017
ReCoSoC 2016	Special Session Co-Chair	11th International Symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC 2016), Special Session on Emerging Technologies for Reconfigurable Systems in the Manycore Era, June 27-29, 2016, Tallinn, Estonia
Computing Frontiers 2016	Publicity Chair	Computing Frontiers, Como, Italy, May 16-18, 2016
NOCS 2016	Publicity Chair	10th International Symposium on Networks-on-Chip, Nara, Japan, Aug 31-Sep 2, 2016
NOCS 2015	Publicity Chair	9th International Symposium on Networks-on-Chip, Vancouver, Canada, Sept. 28-30, 2015
IGSC 2015	Publicity Chair	6th International Green and Sustainable Computing Conference. Las Vegas, Nevada, USA on November 18 - 20, 2015
PDP-2015	Publicity Chair	23rd Euromicro International Conference on Parallel, Distributed and Network-based Processing, Turku, Finland, March 4-6, 2015
NOCS 2014	Publicity Chair	8th International Symposium on Networks-on-Chip, Ferrara, Italy, Sept. 17.19, 2014
ESTIMedia 2013	TPC Chair	11th IEEE Symposium on Embedded Systems for Real-Time Multimedia, Montreal, Canada, Oct. 2013
DATE 2013	Architectures Posters Session Chair	Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools and Applications, 18-22 March 2013, Grenoble, France
ESTIMedia 2012	TPC Co-Chair	10th IEEE Symposium on Embedded Systems for Real-Time Multimedia, Vancouver, Canada, Oct. 2012
DATE 2012	Architectures Posters Session Chair	Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools and Applications, 12-16 March 2012, Dresden, Germany
NOCS 2012	Publicity Chair	Sixth ACM/IEEE International Symposium on Networks-on-Chip, May 9-11, 2012 Copenhagen, Denmark
DTIS 2011	Session Chair	Design and Technology of Integrated Systems in

		Nanoscale Era, 6-8 April 2011, Athens, Greece
DATE 2011	Session Chair	Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications, 14-18 March 2011, Grenoble, France
NOCS 2011	Publicity Chair	Fifth ACM/IEEE International Symposium on Networks-on-Chip, May 1-4, 2011, Pittsburgh, Pennsylvania, USA
INA-OCMC 2011	Publicity Chair	Interconnection Network Architecture: On-Chip, Multi-Chip, January 23th., 2011. Heraklion, Greece

Program Committees

VLSID 2022	International Conference on VLSI Design
VLSI-SoC 2021	IFIP/IEEE International Conference on Very Large Scale Integration
ICCS 2021	International Conference on Circuits and Systems
CEESD 2021	International Conference on Environmental Engineering and Sustainable Development
ICPADS 2020	IEEE International Conference on Parallel and Distributed Systems
PSGEC 2021	Power System and Green Energy Conference
COINS 2020	IEEE International Conference on Omni-layer Intelligent systems
DAC 2020 DAC 2021	Design Automation Conference
BigDataSE 2020	IEEE International Conference on Big Data Science and Engineering
UPIOT 2019	International Conference on Ubiquitous Power Internet of Things
FC 2019	International Conference on Future Computational Technologies and Applications
ScalCom 2019 ScalCom 2018	IEEE International Conference on Scalable Computing and Communications
MicDAT 2018	International Conference on Microelectronic Devices and Technologies
IGSC 2020 IGSC 2018 IGSC 2017	International Green and Sustainable Computing Conference
VDEC 2017 VDEC 2018 VDEC 2019	International Symposium on VLSI Design and Embedded Computing

ISCA 2017	ACM/IEEE International Symposium on Computer Architecture
SMART 2017	International Conference on Smart Cities, Systems, Devices and Technologies
ICOSST 2016	IEEE International Conference on Open Source Systems and Technologies
EMSA 2017	Conference on Embedded Systems and Applications
DMCC 2016	International Workshop on Dependable Many-Core Computing
PEC 2016 PEC 2017	International Conference on Pervasive and Embedded Computing
MCSoC 2015 MCSoC 2021	IEEE International Symposium on Embedded Multicore/Many-core Systems-on-Chip
HPINI 2014 HPINI 2015 HPINI 2016	International Workshop on High Performance Interconnection Networks
Euro-Par 2014	International Conference on Parallel Processing
IGCS 2015 IGCS 2016	International Green and Sustainable Computing Conference
IGCC 2014	International Green Computing Conference
VLSI 2014	International Conference on VLSI Design
EUC 2013	IEEE/IFIP International Conference on Embedded and Ubiquitous Computing
PDP-2013 PDP-2014 PDP-2015	Euromicro International Conference on Parallel, Distributed and Network-Based Computing
NOCS 2012 NOCS 2013 NOCS 2014 NOCS 2015 NOCS 2016 NOCS 2017 NOCS 2018 NOCS 2019 NOCS 2021	ACM/IEEE International Symposium on Networks-on-Chip
INA-OCMC 2011 INA-OCMC 2012	International Workshop on Interconnection Network Architectures: On-Chip, Multi-Chip

INA-OCMC 2013 INA-OCMC 2014 INA-OCMC 2015	
FGCT 2012	First International Conference on Future Generation Communication Technologies
NPC 2011	IFIP International Conference on Network and Parallel Computing
NBiS 2011	International Conference on Network-Based Information Systems
DATE 2011	IEEE/ACM Design and Test in Europe Conference [topic D8 (Networks-on-Chip)]
RTAS 2010	IEEE Real-Time and Embedded Technology and Applications Symposium
CODES+ISSS 2008 CODES+ISSS 2009 CODES+ISSS 2010 CODES+ISSS 2011 CODES+ISSS 2012 CODES+ISSS 2013 CODES+ISSS 2014 CODES+ISSS 2015 CODES+ISSS 2016 CODES+ISSS 2017	IEEE/ACM International Conference on Hardware-Software Codesign and System Synthesis
ESTIMedia 2008 ESTIMedia 2009 ESTIMedia 2010 ESTIMedia 2011 ESTIMedia 2016 ESTIMedia 2017	IEEE Workshop on Embedded Systems for Real-Time Multimedia
SOCC 2008 SOCC 2009 SOCC 2010 SOCC 2011 SOCC 2012 SOCC 2013 SOCC 2014 SOCC 2015 SOCC 2016 SOCC 2017 SOCC 2018 SOCC 2019 SOCC 2020 SOCC 2021	IEEE International SOC Conference
VLSI 2009	International Conference on VLSI Design

ISC 2008 ISC 2009 ISC 2010	Industrial Simulation Conference
SITIS 2009 SITIS 2010 SITIS 2011 SITIS 2012 SITIS 2016 SITIS 2017 SITIS 2018	IEEE/ACM International Conference on Signal-Image Technology & Internet-Based Systems
MELECON 2010	IEEE Mediterranean Electrotechnical Conference
SD4RCES 2010 SD4RCES 2011	SD4RCES Workshop
FCST 2011	International Conference on Frontier of Computer Science and Technology
HPIN 2013	IEEE International Workshop on High Performance Interconnection Networks
EUC 2013	IEEE/IFIP Technical Track on System/Network-on-Chip for the Embedded and Ubiquitous Computing

Editorial Board

- Associate Editor, International Journal of Research Studies in Computer Science and Engineering, 2018-present
- Associate Editor, Global Journals, 2016-present
- Associate Editor, Journal of Low Power Electronics and Applications, 2016-present
- Associate Editor, International Journal on Advanced Research in Science, Engineering and Technology, 2016-2019
- Associate Editor, ICTACT Journal on Micro-Electronics, 2014-present
- Associate Editor, Engineering Science Letters, 2014-2019
- Associate Editor, STM Journal, Recent Trends in Parallel Computing, 2014-present
- Associate Editor, Advances in Electrical Engineering, Hindawi, 2013-2017
- Associate Editor, Computers and Electrical Engineering, Elsevier, 2012-2016
- Associate Editor, Conference Papers in Engineering, Computer Engineering section, 2012-present
- Associate Editor, VLSI Design Journal, Hindawi, 2007-2016
- Associate Editor, Computer Science Journals, 2010-present

Publications

Books

1. Maurizio Palesi and Masoud Daneshtalab. Routing Algorithms in Networks-on-Chip. Springer. ISBN 978-1-4614-8273-4.

Journals

1. Enrico Russo, Maurizio Palesi, Salvatore Monteleone, Davide Patti, Andrea Mineo, Giuseppe Ascia, Vincenzo Catania. "DNN Model Compression for IoT Domain Specific Hardware Accelerators," in IEEE Internet of Things Journal, doi: 10.1109/JIOT.2021.3111723.
2. Nizar Dahir, Ammar Karkar, Maurizio Palesi, Terrence Mak, Alex Yakovlev. Power Density Aware Application Mapping in Mesh-Based Network-on-Chip Architecture: An Evolutionary Multi-Objective Approach. Integration, the VLSI Journal, Elsevier, vol. 81, 2021.
3. Abhijit Das, Abhishek Kumar, John Jose, Maurizio Palesi. Opportunistic Caching in NoC: Exploring Ways to Reduce Miss Penalty. IEEE Transactions on Computers, vol. 70, no. 6, pp. 892-905, 2021.
4. Abhijit Das, Abhishek Kumar, John Jose, Maurizio Palesi. Revising NoC in Future Multi-Core based Consumer Electronics for Performance. IEEE Consumer Electronics Magazine, doi: 10.1109/MCE.2021.3062001.
5. Lahdhiri, H.; Lorandel, J.; Monteleone, S.; Bourdel, E.; Palesi, M. Framework for Design Exploration and Performance Analysis of RF-NoC Manycore Architecture. J. Low Power Electron. Appl. 2020, 10, 37.
6. D. Deb, J. Jose, M. Palesi. COPE: Reducing Cache Pollution and Network Contention by Inter-tile Coordinated Prefetching in NoC based MPSoCs. ACM Transactions on Design Automation of Electronic Systems, 26(326), Feb. 2021.
7. S. Xiao, X. Wang, M. Palesi, A. K. Singh, L. Wang and T. Mak. On Performance Optimization and Quality Control for Approximate-communication-enabled Networks-on-Chip. IEEE Transactions on Computers, 70(11), pp. 1817-1830, Nov. 2021.
8. S. Morteza Nabavinejad, M. Baharloo, K. C. Chen, M. Palesi, T. Kogel, and M. Ebrahimi. An Overview of Efficient Interconnection Networks for Deep Neural Network Accelerators. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2020.
9. S. Mnejja, Y. Aydi, M. Abid, S. Monteleone, V. Catania, M. Palesi, D. Patti. Delta Multi-stage Interconnection Networks for Scalable Wireless On-Chip Communication. Accepted in MDPI Electronics Journal.
10. V. Catania, S. Monteleone, M. Palesi, D. Patti. Impact of Users' Beliefs in Text-Based Linguistic Interaction. IEEE Access vol. 8, pp. 46861-46867, 2020.
11. G. Ascia, V. Catania, S. Monteleone, M. Palesi, D. Patti, J. Jose, V. M. Salerno. Exploiting Data Resilience in Wireless Network-on-ChipArchitectures. ACM Journal on Emerging Technologies in Computing Systems, 16(2), 2020.
12. A. Monemi, F. Khunjush, M. Palesi, H. Sarbazi-Azad. An Enhanced Dynamic Weighted Incremental Technique for QoS Support in NoC. Accepted for publication in ACM Transactions on Parallel Computing.
13. D. Deb, J. Jose, M. Palesi. ECAP:Energy Efficient CAching for Prefetch Blocks in Tiled Chip MultiProcessors. IET Computers & Digital Techniques. 2019.
14. S. Khan, S. Anjum, U. A. Gulzari, M. K. Afzal, F. Ishmanov, M. Palesi. An Optimized Hybrid Algorithm in term of Energy and Performance for Mapping Real Time

Workloads on 2D based On-Chip Networks. Applied Intelligence. Vol. 48, Issue 12, pp. 4792--4804, December 2018.
15. M. Tang, J. Lin, M. Palesi. The Suboptimal Routing Algorithm for 2D Mesh Network. IEEE Transactions on Computers. Vol. 67, no. 5, pp. 704-716, May 2018.
16. V. Catania, A. Mineo, S. Monteleone, M. Palesi, D. Patti. Improving Energy Efficiency in Wireless Network-on-Chip Architectures. ACM Journal on Emerging Technologies in Computing Systems. Volume 14 Issue 1, March 2018.
17. A. Monemi, C. Y. Ooi, M. Palesi, M. N. Marsonoa. Ping-Lock Round Robin Arbiter. Microelectronics Journal, Microelectronics Journal. Vol. 63, No. 1, pp. 81-93, May 2017.
18. A. Monemi, J. W. Tang, M. Palesi, M. N. Marsono. ProNoC: A Low Latency Network-on-Chip based Many-Core System-on-Chip Prototyping Platform., Microprocessors and Microsystems, Elsevier, 54, pp. 60-74, 2017.
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